



UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
-----------------	-------------	----------------------	---------------------	------------------

10/631,160

07/31/2003

James R. Peterson

200207081-1

7545

22879

7590

11/02/2006

HEWLETT PACKARD COMPANY
P O BOX 272400, 3404 E. HARMONY ROAD
INTELLECTUAL PROPERTY ADMINISTRATION
FORT COLLINS, CO 80527-2400

EXAMINER

PATEL, NIKETA I

ART UNIT

PAPER NUMBER

2181

DATE MAILED: 11/02/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary

Application No.

10/631,160

Applicant(s)

PETERSON ET AL.

Examiner

Niketa I. Patel

Art Unit

2181

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 08 August 2006.
- 2a) ☒ This action is **FINAL**. 2b) ☐ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1,3-6 and 8-19 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 1,3-6 and 8-19 is/are rejected.
- 7) ☐ Claim(s) _____ is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☒ The drawing(s) filed on 31 July 2003 is/are: a) ☒ accepted or b) ☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some * c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
 2. ☐ Certified copies of the priority documents have been received in Application No. _____.
 3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

FRITZ FLEMING

SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2100**Attachment(s)**

- 1) ☐ Notice of References Cited (PTO-892)
- 2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
- 3) ☐ Information Disclosure Statement(s) (PTO/SB/08)
Paper No(s)/Mail Date _____

- 4) ☐ Interview Summary (PTO-413)
Paper No(s)/Mail Date. 10/29/2006
- 5) ☐ Notice of Informal Patent Application
- 6) ☐ Other: _____

DETAILED ACTION

Claim Rejections - 35 USC § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(e) The invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

2. As far as the examiner can interpret the claims in light of the 35 U.S.C. 112, second paragraph, supra claims 1, 3-5 and 6, 8-10, 12-15, 17-19 are rejected under 35 U.S.C. 102(e) as being anticipated by Boyle et al. U.S. Patent Number 6,708,251 B1 (hereinafter "*Boyle*").
3. **Referring to claim 1**, *Boyle* teaches a method and a memory device interface comprising: determining at least one characteristic [see column 3, lines 45-48 and column 7, lines 8-19] of a first input/output (I/O) device [see figure 2, element 22 and column 4, lines 32-60] that is coupled to a memory device interface [see figure 2, element 80], the memory device interface being configured to enable data transfers between the I/O device and a memory device [see column 7, lines 37-43 'transfers'] and buffering data corresponding to the first I/O device in a first portion of a buffer of the memory device interface [see figure 2, element 41], a size of the first portion being responsive to the at least one characteristic of the first I/O device [see column 7, lines 5-19, 37-43, 59-62]; determining at least one characteristic [see column 3, lines 54-62 and column 7, lines 8-19] of a second I/O device [see figure 2, element 24] that is coupled to the memory device interface [see figure 2, element 80]; and buffering data corresponding to the second I/O device in a second portion of the buffer [see figure 2, element 42], a size of the

Art Unit: 2181

second portion being responsive to the at least one characteristic of the second I/O device [see column 7, lines 5-19, 37-43, 59-62 and column 4, lines 32-60, which discloses that the system 20 differentiates element 22 and 24 from each other and that the host device can comprises a set-top box, a personal video recorder or other source of audiovisual information, this differentiation is made by determining a characteristic of both of the elements 22 and 24.]

4. **Referring to claim 6**, *Boyle* teaches a method for allocating buffer capacity in a memory device interface that is configured to transfer data between an input/output (I/O) device and a memory device [see figure 2, elements 22, 24, 40, 50, 70], the method comprising: buffering data received via a first data transfer link [see figure 2, element 52] in a first portion of a buffer of the memory device interface [see figure 2, element 41]; buffering data received via a second data transfer link [see figure 2, element 72,74] in a second portion of the buffer [see figure 2, element 42], a buffering capacity of the first portion being different than a buffering capacity of the second portion [see column 5, lines 9-34, compressed and uncompressed data and lines 53-65, IT data and column 6, lines 35-44]; and wherein the buffering capacity of the first portion is responsive to at least one characteristic of a first I/O device that provides data to the memory device interface via the first data transfer link [see column 7, lines 5-19, 37-43, 59-62 and column 4, lines 32-60, which discloses that the system 20 differentiates element 22 and 24 from each other and that the host device can comprises a set-top box, a personal video recorder or other source of audiovisual information, this differentiation is made by determining a characteristic of both of the elements 22 and 24], and the buffering capacity of the second portion is responsive to at least one characteristic of a second I/O device that provides data to the memory device interface via the second data transfer link [see column 7, lines 5-19, 37-43, 59-62

and column 4, lines 32-60, which discloses that the system 20 differentiates element 22 and 24 from each other and that the host device can comprises a set-top box, a personal video recorder or other source of audiovisual information, this differentiation is made by determining a characteristic of both of the elements 22 and 24.]

5. **Referring to claim 10**, *Boyle* teaches a memory device interface that is configured to enable data transfers between an input/output (I/O) device, the memory device interface comprising: a buffer [see figure 2, element 40]; a first plurality of registers that are configured to enable the memory device interface to buffer in a first portion of the buffer data corresponding to a first I/O device [see figure 2, element 41]; and a second plurality of registers that are configured to enable the memory device interface to buffer in a second portion of the buffer data corresponding to a second I/O device [see figure 2, element 42], a size of the first portion of the buffer being different than a size of the second portion of the buffer [see column 6, lines 35-44; column 7, lines 5-19, 37-43, 59-62 and column 4, lines 32-60, which discloses that the system 20 differentiates element 22 and 24 from each other and that the host device can comprises a set-top box, a personal video recorder or other source of audiovisual information, this differentiation is made by determining a characteristic of both of the elements 22 and 24.]

6. **Referring to claim 15**, *Boyle* teaches a memory device interface comprising: a buffer [see figure 2, element 40]; a first plurality of registers that are configured to enable the memory device interface to buffer in a first portion of the buffer data received via a first data transfer link [see figure 2, element 41, 52, 22]; and a second plurality of registers that are configured to enable the memory device interface to buffer in a second portion of the buffer data received via a second data transfer link [see figure 2, element 42, 72, 74, 24], a size of the first portion of the

Art Unit: 2181

buffer being different than a size of the second portion of the buffer [see column 6, lines 35-44; column 7, lines 5-19, 37-43, 59-62 and column 4, lines 32-60, which discloses that the system 20 differentiates element 22 and 24 from each other and that the host device can comprises a set-top box, a personal video recorder or other source of audiovisual information, this differentiation is made by determining a characteristic of both of the elements 22 and 24.]

7. **Referring to claim 19**, *Boyle* teaches a system comprising: means for determining at least one characteristic of a first input/output (I/O) device that is coupled to a memory device interface [see column 6, lines 35-44; column 7, lines 5-19, 37-43, 59-62 and column 4, lines 32-60, which discloses that the system 20 differentiates element 22 and 24 from each other and that the host device can comprises a set-top box, a personal video recorder or other source of audiovisual information, this differentiation is made by determining a characteristic of both of the elements 22 and 24], the memory device interface being configured to enable data transfers between the I/O device and a memory device [see column 4, lines 32-60; column 6, lines 35-44; column 7, lines 5-19, 37-43, 59-62]; means for buffering data corresponding to the first I/O device in a first portion of a buffer of the memory device interface, a size of the first portion being responsive to the at least one characteristic of the first I/O device [see column 4, lines 32-60; column 6, lines 35-44; column 7, lines 5-19, 37-43, 59-62]; means for determining at least one characteristic of a second I/O device that is coupled to the memory device interface [see column 4, lines 32-60; column 6, lines 35-44; column 7, lines 5-19, 37-43, 59-62]; and means for buffering data corresponding to the second I/O device in a second portion of the buffer, a size of the second portion being responsive to the at least one characteristic of the second I/O device [see column 4, lines 32-60; column 6, lines 35-44; column 7, lines 5-19, 37-43, 59-62.]

8. **Referring to claims 3, 7, 17,** *Boyle* teaches further comprising: receiving data from the first I/O device via a first data transfer link [see figure 2, element 52]; and receiving data from the second I/O device via a second data transfer link [see figure 2, element 72, 74.]
9. **Referring to claims 4, 8,** *Boyle* teaches further comprising: receiving a first data unit from the first I/O device [see column 7, lines 5-43]; buffering the first data unit in the first portion of the buffer, and transferring the first data unit to the memory device [see column 7, lines 5-43], receiving a second data unit from the second I/O device [see column 7, lines 5-43], buffering the second data unit in the second portion of the buffer, and transferring the second data unit to the memory device [see column 7, lines 5-43.]
10. **Referring to claim 5,** *Boyle* teaches wherein the at least one characteristic comprises at least one of: a rate at which the I/O device is able to read data from the memory device, a rate at which the I/O device is able to write data to the memory device; a bandwidth of a link coupled between the I/O device and the memory device interface, a size of a data unit that the I/O device reads from the memory device per read request a size of a data unit that the I/O device writes to the memory device per write request, a tolerance that the I/O device has for a delay by the memory device interface in fulfilling a write request; or a tolerance that the I/O device has for a delay by the memory device interface in fulfilling a read request [see column 7, lines 5-19, 37-43, 59-62 – ‘large amount of data to be transferred’, ‘small amount of data to be transferred’, ‘bandwidth’, ‘buffer demands’.]
11. **Referring to claims 9,** *Boyle* teaches further comprising: receiving a first data unit from the memory device; buffering the first data unit in the first portion of the buffer [see column 7, lines 5-43]; transferring the first data unit to the first I/O device [see column 7, lines 5-43];

Art Unit: 2181

receiving a second data unit from the memory device; buffering the second data unit in the second portion of the buffer [see column 7, lines 5-43]; and transferring the second data unit to the second I/O device [see column 7, lines 5-43.]

12. Referring to claims 12, 18, *Boyle* teaches wherein the plurality of registers comprises: a first buffer allocation counter that specifies a buffer allocation value that is configured to enable data received from the first I/O device to be buffered in the first portion of the buffer see column 6, lines 49-55, 'a chip or a circuit that allocates buffer memory 40' and column 7, lines 5-19]; and a second buffer allocation counter that specifies a buffer allocation value that is configured to enable data received from the second I/O device to be buffered in the second portion of the buffer [see column 6, lines 49-55, 'a chip or a circuit that allocates buffer memory 40' and column 7, lines 5-19.]

13. Referring to claims 13, 14, *Boyle* teaches wherein the value of the first buffer allocation counter is decremented response to a buffer allocation value being sent to the first I/O device [see column 6, lines 49-55, 'a chip or a circuit that allocates buffer memory 40' and column 7, lines 5-43]; wherein the value of the first buffer allocation counter is incremented responsive to data being read from the first portion of the buffer [see column 6, lines 49-55, 'a chip or a circuit that allocates buffer memory 40' and column 7, lines 5-43.]

Claim Rejections - 35 USC § 103

14. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are

Art Unit: 2181

such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

15. Claims 11, 16 are rejected under 35 U.S.C. 103(a) as being unpatentable over *Boyle* and further in view of Ward et al. U.S. Patent Number: 4,894,770 (hereinafter "*Ward*".)

16. Referring to claims 11, 16, *Boyle* teaches buffer memory [see figure 2, element 40] however does not set forth the limitation of wherein the buffer comprises random access memory (RAM) however, *Ward* teaches a buffer comprising random access memory.

It would have been obvious to one of ordinary skill in the art at the time of applicant's invention that it was old and well known in the computer art to get the advantage of the ability of accessing data in random order by implementing the buffer using RAM, as disclosed by *Ward* [see column 1, lines 9-32.] It would have been obvious to one of ordinary skill in the art at the time of applicant's invention to implement the buffer using RAM to get this advantage.

Response to Arguments

17. Applicant's arguments filed 08/08/2006 have been fully considered but they are not persuasive. The applicant argues that (1) *Boyle* does not teach the limitation of "determining at least one characteristic of a second I/O device that is coupled to the memory device interface; and buffering data corresponding to the second I/O device in a second portion of the buffer, a size of the second portion being responsive to the at least one characteristic of the second I/O device", at pages 7-11 of the remarks section (2) that the rejection of claims 6, 10, 15 and 19 is improper since the Office Action failed to address these claims individually.

The examiner respectfully disagrees with these arguments.

As per the first argument, *Boyle* teaches the limitation of determining at least one characteristic [see column 3, lines 54-62 and column 7, lines 8-19] of a second I/O device [see figure 2, element 24 and column 4, lines 32-60, which discloses that the system 20 differentiates element 22 and 24 from each other and that the host device can comprises a set-top box, a personal video recorder or other source of audiovisual information, this differentiation is made by determining a characteristic of both of the elements 22 and 24] that is coupled to the memory device interface [see figure 2, element 80]; and buffering data corresponding to the second I/O device in a second portion of the buffer [see figure 2, element 42], a size of the second portion being responsive to the at least one characteristic of the second I/O device [see column 7, lines 5-19, 37-43, 59-62.]

As per the first argument, the examiner has individually addressed each of the claims 6, 10, 15 and 19 to ease the applicant's burden.

Conclusion

18. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event,

Art Unit: 2181


however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Niketa I. Patel whose telephone number is (571) 272 4156. The examiner can normally be reached on M-F 8:00 A.M. to 5:00 P.M.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Fritz Fleming can be reached on (571) 272 4145. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

NP
10/16/2006


FRITZ FLEMING
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2100
10/29/2006